Abstract

The present invention provides a CAM (content addressable memory) apparatus having: a first memory device (10) with a word line input (WL) and at least one storage node (12; 13) for storing a first bit of a data word; a second memory device (11) with a word line input (WL) and at least one storage node (14; 15) for storing a second bit of a data word; and a comparator device (16) for comparing the first and second stored bits with two precoded comparison bits fed via four inputs (20; 21; 22; 23) and for driving a hit node (17) in the event of the first stored bit corresponding to the first comparison bit and the second stored bit corresponding to the second comparison bit.

Figure 1